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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,855	04/09/2004	Min-Lung Huang	HUAN3262/EM	8687

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,855	HUANG, MIN-LUNG	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In lines 1-3 of claim 14, the limitation, "wherein the first electrically conductive layer comprises a titanium layer, an aluminum layer, a nickel-vanadium alloy and a copper layer," is not enabling because the specification does not clearly or specifically describe an electrically conductive layer comprising a four layer structure of a titanium layer, an aluminum layer, a nickel-vanadium layer, and a copper layer. For examination purposes, the Office will interpret claim 14 to mean that the first electrically conductive layer comprises a titanium layer, wherein the titanium layer is directly attached to the bonding pads.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 8-10, 13, 14 and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by **Greer (US 2003/0013290)**.

With respect to **claim 8, Greer** teaches **(FIGS. 1-5)** a semiconductor wafer applicable to a flip chip device, comprising:

an active surface **(the substrate 100 contains an active device with doped regions 104 and a gate electrode 110) (pg. 2: [0015]**;

a plurality of bonding pads **(128 or 202)** formed on the active surface **(pg. 2: [0018])**;

a passivation **(300)** covering the active surface and exposing the bonding pads **(128) (pg. 1: [0013], pg. 2: [0019])**;

a first electrically conductive layer **(402)** formed on the bonding pads **(128) (pg. 2: [0020])**;

and a second electrically conductive layer **(404, including the nickel and tin intermetallics formed at the surface of 404; pg. 3: [0029])** formed on the first electrically conductive layer **(402)**, wherein the second electrically conductive layer comprises tin and nickel **(pg. 3: [0027], [0029])**.

With respect to **claim 9, Greer** teaches the semiconductor wafer of claim 8, as set forth above, further comprising a plurality of bumps **(502; pg. 1: [0003], pg. 4: [0031])** formed above the bonding pads **(128)** and attached to the second electrically conductive layer **(pg. 3: [0029])**.

With respect to **claim 10, Greer** teaches the semiconductor wafer of claim 8, as set forth above, wherein the second electrically conductive layer **(404)** is extended above the active surface **(surface of substrate 100) (FIG. 5)**.

With respect to **claim 13, Greer** teaches the semiconductor wafer of claim 8, as set forth above, wherein the first electrically conductive layer **(402)** is titanium **(pg. 3: [0023])**.

With respect to **claim 14, Greer** teaches the semiconductor wafer of claim 8, as set forth above, wherein the first electrically conductive layer **(402)** comprises a titanium layer which is directly attached to the bonding pads **(128 or 202) (pg. 2: [0020]; pg. 3: [0023])**.

With respect to **claim 16, Greer** teaches the semiconductor wafer of claim 8, as set forth above, wherein the quantity of tin is less than the quantity of nickel **(Ni_3Sn; pg. 3: [0027])**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-4, 6 and 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicant's Admitted Prior Art (AAPA)** in view of **Andricacos et al. (US 6,224,690)**.

With respect to **claim 1, AAPA** teaches **(pg. 2: [0004]-[0005])** an under bump metallization structure **(FIG. 1)** applicable to be disposed on bonding pads **(104)** of a semiconductor wafer **(101)**, wherein a passivation layer **(102)** covers the wafer and exposes the bonding pads **(104)**, the under bump metallization structure **(106)** comprising:

an adhesive layer **(106a)** formed on the bonding pads **(104)**;

a first barrier layer **(106b)** disposed on the adhesive layer **(106a)**; and

a wetting layer formed **(106c)** on the first barrier layer **(106b)**.

Thus, **AAPA** teaches all the limitations of the claim with the exception of disclosing: a second barrier layer disposed on the wetting layer wherein a material of the second barrier comprises tin and nickel.

However, **Andricacos** teaches a under bump metallization structure **(FIG. 4)**, wherein a second barrier layer of nickel-tin intermetallic **(col. 5: lns. 26-32)** is disposed on the wetting layer **(Cu)**.

With respect to **claim 2, Andricacos** teaches wherein the quantity of the tin is smaller than the quantity of the nickel **(this is implicit because Andricacos states that although a nickel-tin intermetallic is formed, the under bump metallization does not spall off; col. 5: lns. 26-32)**.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of **AAPA** with the teaching of **Andricacos**, to form a barrier layer on the wetting layer of copper, for the purpose of preventing the reaction of the solder with the underlying copper, and thus preventing the spalling of the under bump metallization layer **(col. 5: lns. 26-32)**.

With respect to **claim 3, AAPA and Andricacos** teaches the under bump metallization structure of claim 1, as set forth above. Furthermore, **AAPA** teaches wherein the first barrier layer comprises nickel-vanadium or nickel **(pg. 2: [0005])**.

With respect to **claim 4, AAPA and Andricacos** teaches the under bump metallization structure of claim 1, as set forth above. Furthermore, **AAPA** teaches wherein the wetting layer is a copper layer **(pg. 2: [0005])**.

With respect to **claim 6, AAPA and Andricacos** teaches the under bump metallization structure of claim 1, as set forth above. Furthermore, **AAPA** teaches wherein the adhesive layer comprises titanium **(pg. 2: [0005])**.

With respect to **claim 7, AAPA and Andricacos** teaches all the limitations of the claim, as set forth above in claim 1, with exception of explicitly disclosing: wherein the thickness of the second barrier layer is ranged from about 50 μm to about 80 μm.

However, it would have obvious to one of ordinary skill in the art to form the second barrier layer with a thickness ranging from about 50 μm to about 80 μm, because absent evidence of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955).

4. **Claims 11, 12, 15 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Greer (US 2003/0013290)**, as applied to claim 8 above, and further in view of **Kuwabara et al. (US 6,707,153)**.

With respect to **claim 11, Greer** teaches all the limitations of the claim, as set forth above in claim 8, with the exception of disclosing: a dielectric layer covering the second electrically conductive layer and exposing a portion of the second electrically conductive layer to form a redistributed pad.

However, **Kuwabara** teaches a semiconductor wafer comprising a dielectric layer **(100)** covering a plurality of conductive layers **(20)** and exposing a potion of the conductive layers to form a redistributed pad **(22) (FIG. 1; col. 6: lns. 24-41 and lns. 63-67)**.

With respect to **claim 12, Kuwabara** further teaches a bump **(30)** formed on the redistributed pad **(22) (FIG. 1; col. 6: lns. 37-41)**.

With respect to **claim 15, Kuwabara** also teaches wherein a material of the dielectric layer **(100)** comprises polyimide **(col. 6: lns. 52-55 and 63-67; Kuwabara states that the first resin layer can be formed of polyimide resin and that the second resin layer 100 may be made of the same material as the first resin layer 40)**.

With respect to **claim 18, Kuwabara** also teaches wherein a material of the dielectric layer **(100)** comprises benzocyclobutene **(col. 6: lns. 52-55 and 63-67; Kuwabara states that the first resin layer can be formed of benzocyclobutene**

(BCB) and that the second resin layer 100 may be made of the same material as the first resin layer 40).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of **Greer** with the teaching of **Kuwabara**, to form a dielectric layer of the electrically conductive layers, for the disclosed intended purpose of reducing cracking of the semiconductor wafer and preventing detachment of the semiconductor wafer **(col. 8: lns. 1-12)**.

5. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Greer (US 2003/0013290)**.

With respect to **claim 17, Greer** teaches all the limitations of the claim, as set forth above in claim 11, with the exception of explicitly disclosing: wherein the thickness of the second electrically conductive layer is ranged from about 50 μm to about 80 μm.

However, it would have obvious to one of ordinary skill in the art to form the second electrically conductive layer with a thickness ranging from about 50 μm to about 80 μm, because absent evidence of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955).

Response to Arguments

Applicant's arguments with respect to claims 1-4 and 6-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abul Kalam

THAO X. LE
PRIMARY PATENT EXAMINER